Energy Efficiency of Computing Architectures

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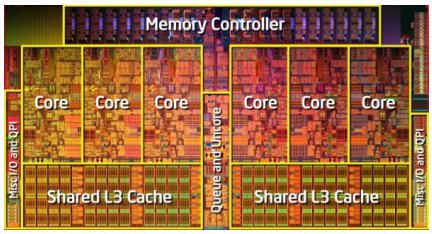
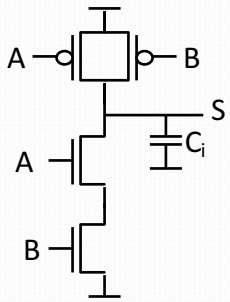
Power Consumption in Silicon Chips

- Chips, logic gates and transistors

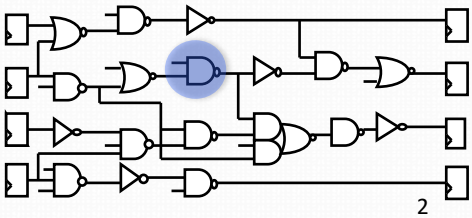


Intel's Xeon Chip



$$P_i = \alpha_i.f_i.C_i.Vdd^2 + I_{leak_i}.Vdd$$

$$P = \sum_i \left[\alpha_i.f_i.C_i.Vdd^2 + I_{leak_i}.Vdd\right]$$



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Outline

- Power and energy consumption basics
- Power consumption in processors
- Multicore: power and utilization walls
- Energy advantages of hardware accelerators
- Playing with accuracy for reducing energy
- Towards heterogeneous manycores
  - 3D stacking
  - Optical interconnect

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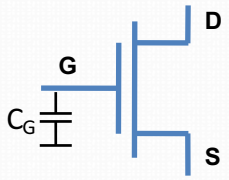
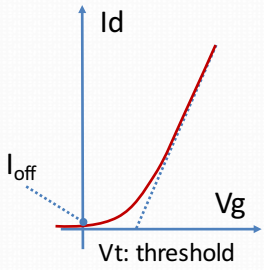
The Basic Element: Transistor

- Transistor as a switch





- Vg > Vt: NMOS on
  - Resistance R_{DS}
- Vg < Vt: NMOS off
  - Leakage I_{off}

- Gate: capacitance C_G
- Switch: resistance R_{DS}

$$R_{DS} \propto \frac{1}{V_{dd} - V_t}$$

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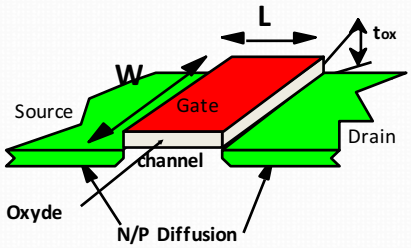
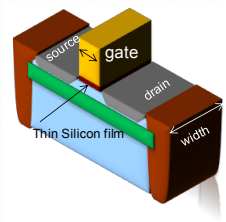
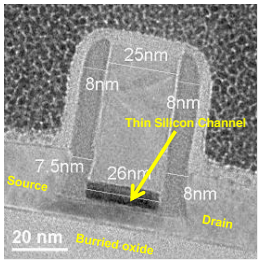
Transistors

- Bulk CMOS



- FD-SOI CMOS
  - STMicroelectronics
  - Vt tuning





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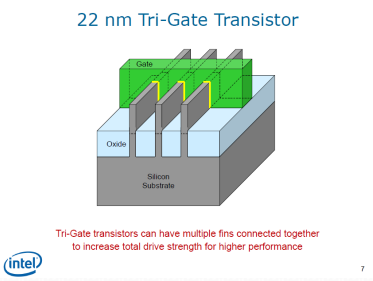
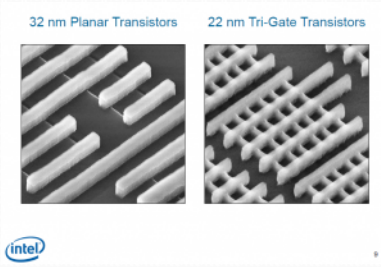
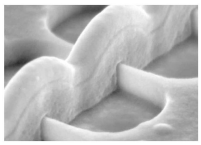
Transistors

- Intel FinFET: transistors go 3D







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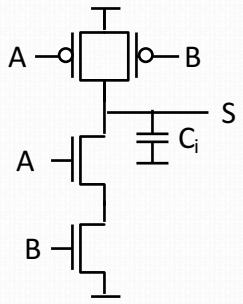
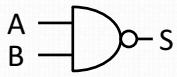
Gates



A	B	S
0	0	1
0	1	1
1	0	1
1	1	0



- Delay of a gate

$$\mathbf{Delay} \propto \mathbf{R_{DS}.C_i} \propto \frac{\text{Relative FanOut}}{V_{dd} - V_t}$$

- Dynamic power

$$\mathbf{P_{dyn_i}} = \alpha_\mathbf{i}.\mathbf{f_{clk}}.\mathbf{C_i}.\mathbf{Vdd^2}$$

- Leakage power

$$\mathbf{P_{stat_i}} = \mathbf{N}.\mathbf{I_{off}}.\mathbf{Vdd}$$

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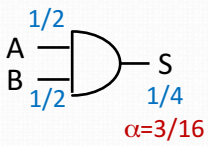
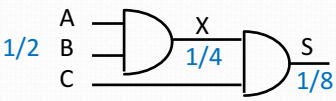
Activity

- Activity α_i is the probability to have a *0→1* transitions at the output of a gate
- Example: AND gate
  - $P_S = P(S=1) = P_A P_B$
  - $\alpha_i = P_S(1- P_S)$



A	B	S
0	0	0
0	1	0
1	0	0
1	1	1

- Activity propagation



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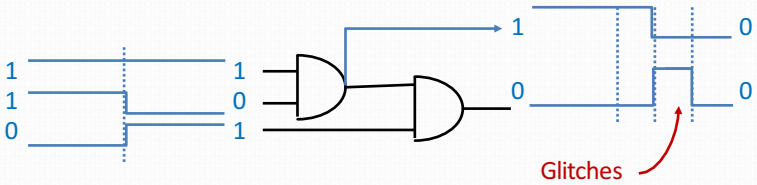
Propagating Activity is not So Simple

- Conditional probabilities

- Glitches: gate delay
  - Significant in arithmetic



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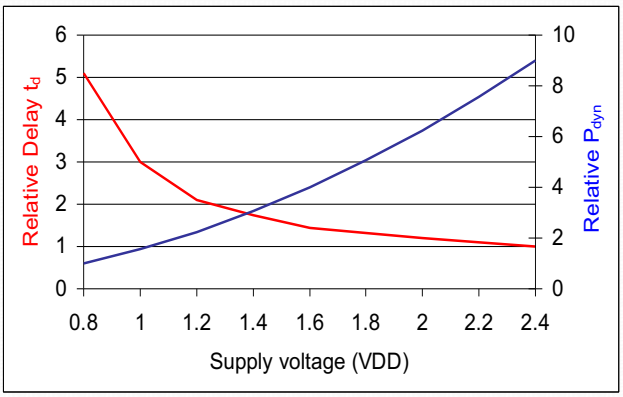
Dynamic Power vs. Performance

- Decreasing Vdd reduces power but increases delay

$$P_{dyn_i} = \alpha_i . f_{clk} . C_i . Vdd^2$$



$$Delay \propto \frac{1}{V_{dd} - V_t}$$

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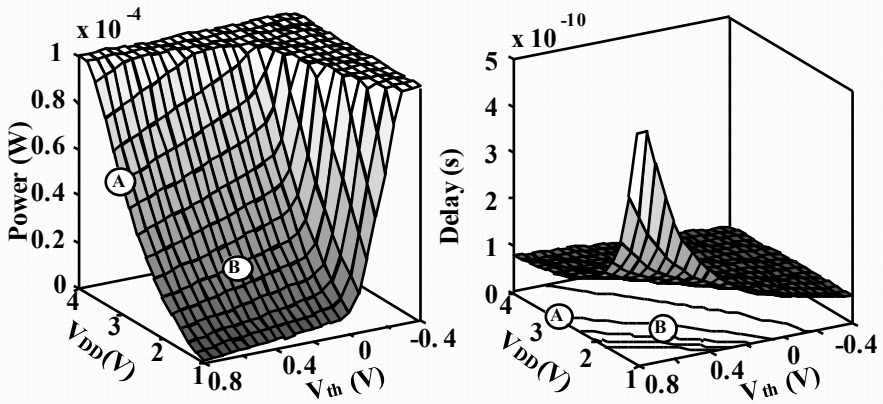
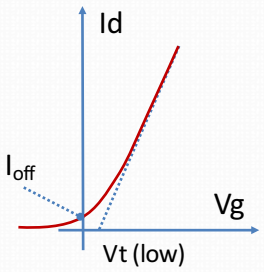
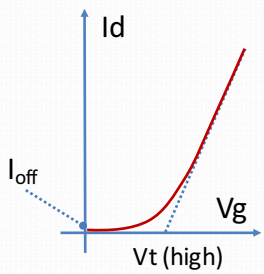
Power Dissipation and Circuit Delay



Leakage vs. performance

- High performance
- Low leakage





$$P_{stat_i} = N.I_{off}.Vdd$$

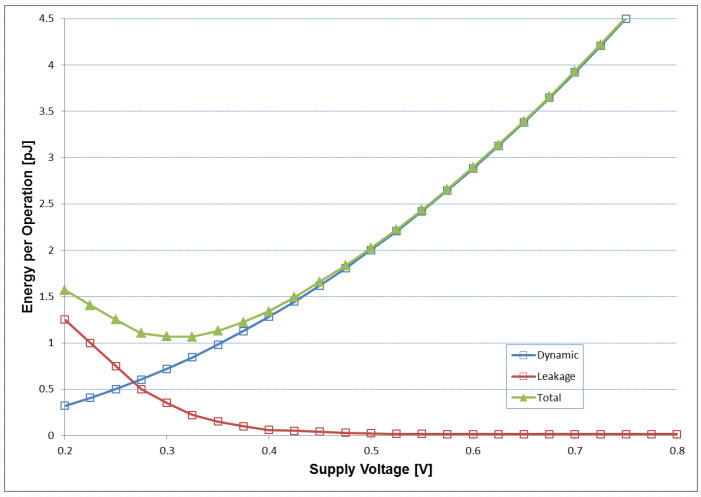
$$Delay \propto \frac{1}{V_{dd} - V_t}$$

Ioff:

- Exponential in inverse of Vt
- Exponential in temperature
- Linear in device count

Minimum Energy per Operation

- Putting all together



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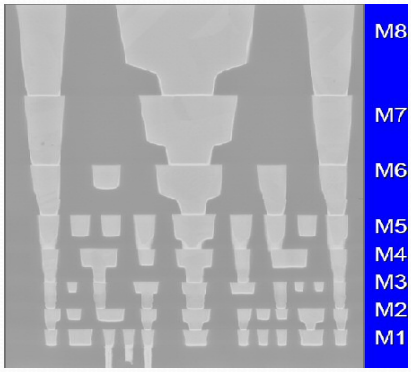
On-Chip Interconnect?

- Gate delay decreases but… wire delay increases
- Crossing chip in 5-10 clock cycles
- Also affected by noise…



- Metal layers to reduce wire delay
- Repeaters
- Towards network-on-chip

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Conclusion: Power in CMOS

$$\mathbf{P} = \sum_{\mathbf{i}} \left[\alpha_{\mathbf{i}}.\mathbf{f}_{\mathbf{i}}.\mathbf{C}_{\mathbf{i}}.\mathbf{Vdd}^{\mathbf{2}} + \mathbf{I}_{\mathbf{leak}_{\mathbf{i}}}.\mathbf{Vdd}\right]$$

- Dynamic power
  - 40-70% today
  - Decreasing relatively
  - DVFS becomes more and more difficult
- Leakage power
  - 20-50 % today
  - Increasing rapidly
    - number of transistors
    - Vdd/Vt scaling
  - Critical for memory

$$P = \frac{energy}{operation} \times rate + static\ power$$

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  - 3D stacking
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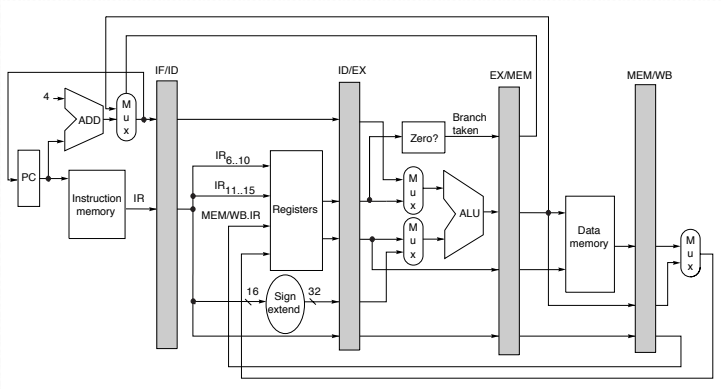
Power Consumption in Processors

- A typical (yet simple) processor pipeline



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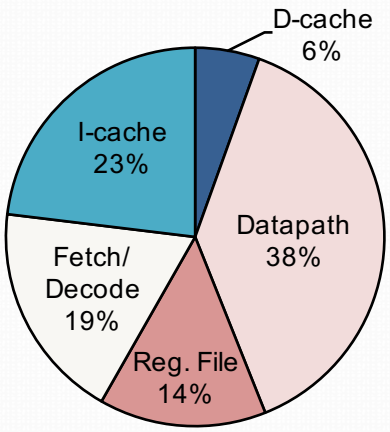
Energy Cost in a Processor



MIPS processor
91 pJ/instr.

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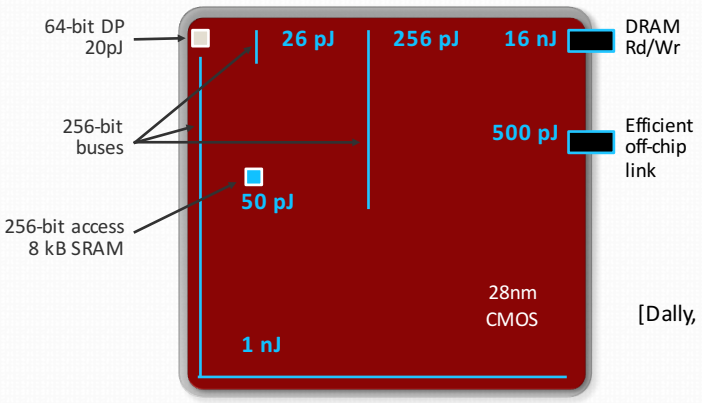
Energy Cost in a Processor

- Fetching operands costs more than computing



[Dally, IPDPS'11]

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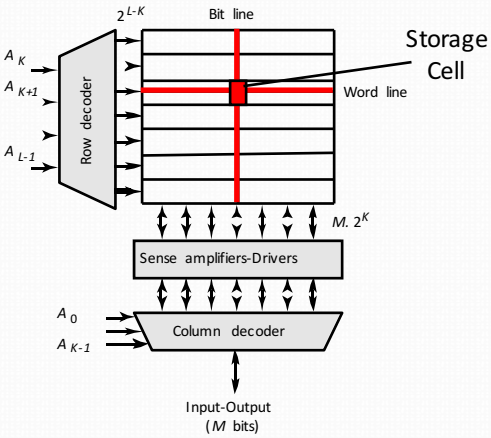
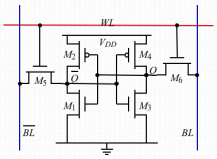
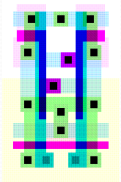
Energy Cost in a Memory

- L2 Cache contains 4 Millions SRAM cells
- Raw/column of 2000 cells







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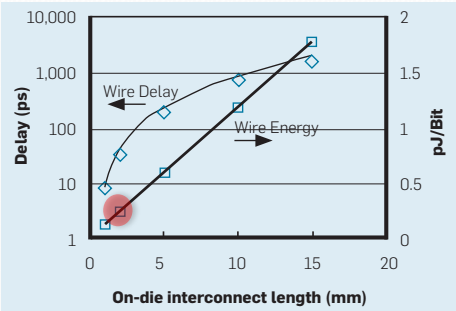
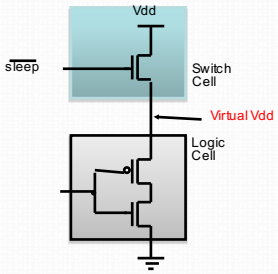
The Energy Cost of Data Movement

- Future processor up to 3 Tera-op/sec
- At minimum requires 64b x 9 Tera-operands to be moved each second
- If on average 1mm (10% of die size) then
  - 0.1pJ/bit x 576 Tbits/s
  - consumes 58 Watts!



Reducing Power

- Power gating, multi-Vt
- Clock gating
- Vdd scaling
  - Parallel, pipeline
- Activity reduction
  - Pre-computation, correlation, encoding
- Glitch Power Reduction



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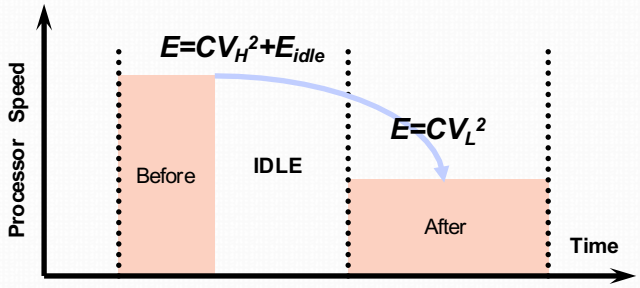
Dynamic Power Management

- Dynamic Voltage and Frequency Scaling (DVFS)
- Reduce speed (clock freq.) and Vdd depending on processor activity



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Outline

- Power and energy consumption basics
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- Multicore: power and utilization walls
- Energy advantages of hardware accelerators
- Playing with accuracy for reducing energy
- Towards heterogeneous manycores
  - Can 3D stacking help?
  - Optical interconnect

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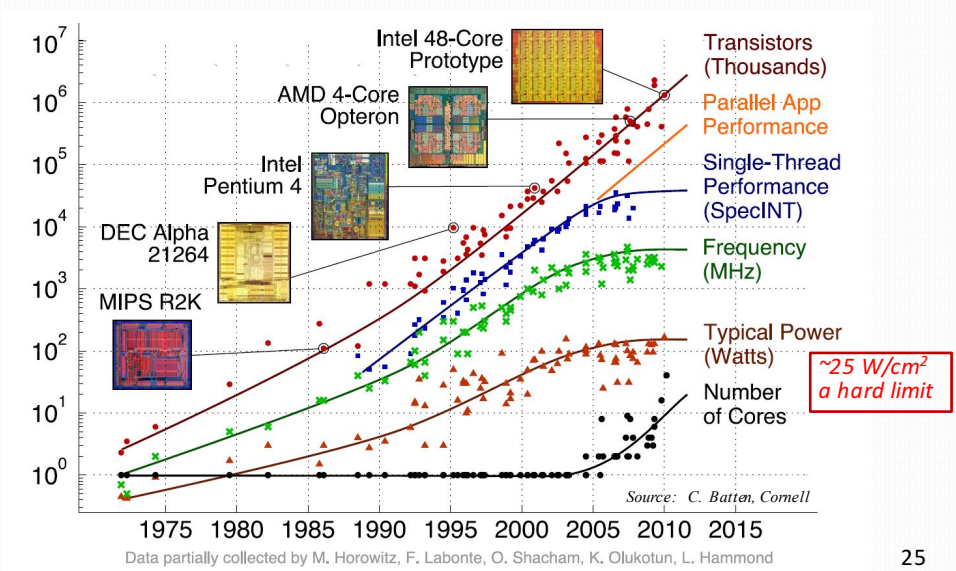
The "Power Wall"



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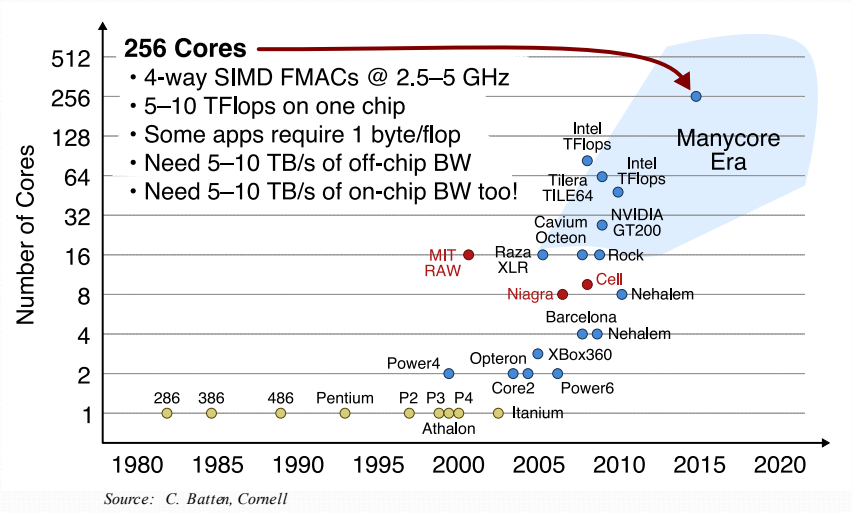
and the "Multicore Era"

- Increasing performance by increasing # of cores



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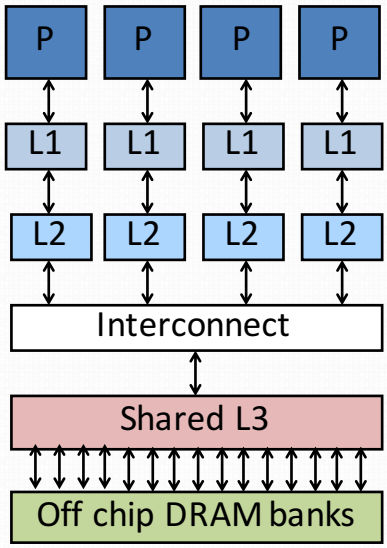
Shared-Memory Multiprocessor



- Processors communicate with shared address space by memory read/write
- Hardware-managed, implicitly-addressed, coherent caches
- Bandwidth depends on
  - Cache size, associativity
  - Replacement policy, coherence protocol
  - Application requirements

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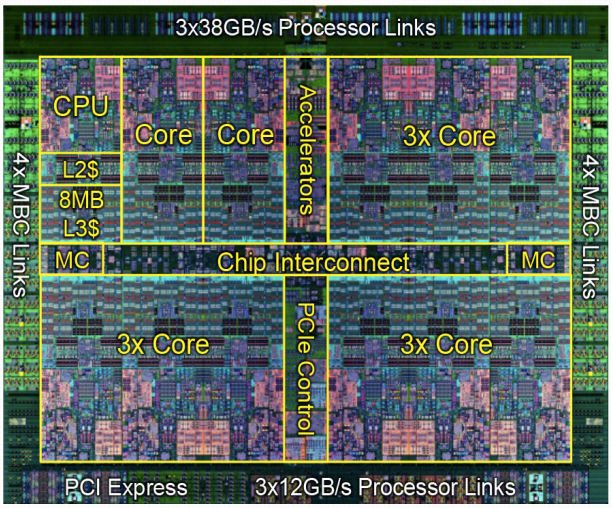
IBM Power 8



- 12 cores (SMT 8)
- 2013 (2015)
- 22nm, 6.5cm^2
- Caches
  - 512 KB SRAM L2 / core
  - 96 MB eDRAM shared L3
  - Up to 128 MB eDRAM L4 (off-chip)

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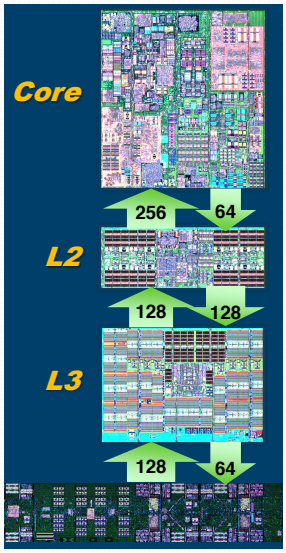
IBM Power 8

- Across 12 core chip
  - 4 TB/sec L2 BW
  - 3 TB/sec L3 BW
- 230 GB/s sustained external memory bandwidth

GB/sec shown assuming 4 GHz



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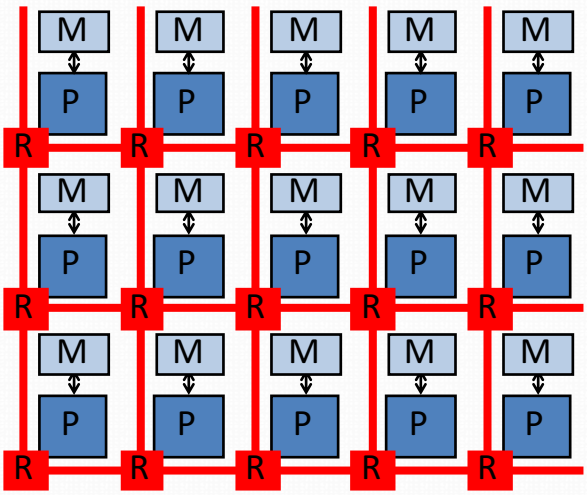
Distributed Memory



- Separate address space for each processor
- Processors communicate via message passing
- Software-managed, explicitly-addressed, local memories
- Sometimes also distributed shared memory

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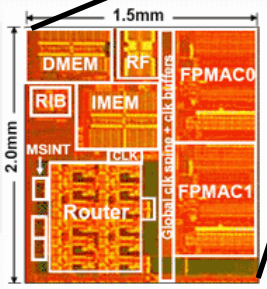
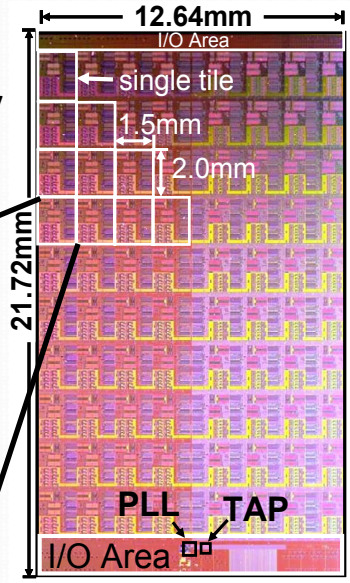
Intel's 80 Core Terascale Processor

- 80 cores (2 FMACs)
- 1.6 SP TFOPS @ 5GHz 1.2V
- 320 GB/s bisection router bandwidth

Routers write directly into memory:

any core could write into the memory of any other core with low latency (2 cycles)





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Moving to multicore

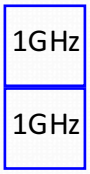
- 1 core@2GHz@1.2V@1W

1W
1.2V

- 1 core@1GHz@0.8V@0.25W

0.22W
0.8V

- 2 cores@1GHz@0.8V@0.5W
- But… twice area (and not so simple)



- Advanced technology nodes?

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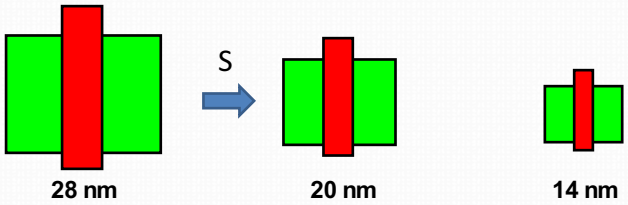
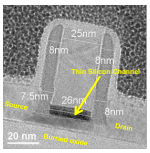
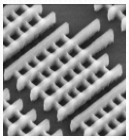
Technology Scaling

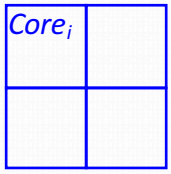




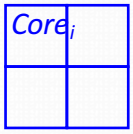


Classical (Dennard's) scaling

Device count	S^2
Device frequency	S
Capacitance, Vdd	1/S
Device power	$1/S^2$
Utilization	**1**



100W@*f*



50W@*1.4.f*

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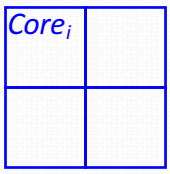
End of Dennard's Scaling

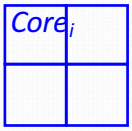
- Energy efficiency is not scaling along with integration capacity

Leakage limited scaling

Device count	S^2
Device frequency	S
Device power (cap)	1/S
Device power (V_{dd})	**~1**
Utilization	**$1/S^2$**



100W@*f*



100W@*1.4.f*
(w/o) leakage

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